CLAIMS

What is claimed is:

1. A method of forming at least a portion of a SONOS dual bit memory core array upon a semiconductor substrate, the method comprising:

forming a portion of a charge trapping dielectric layer over the substrate;

forming a resist over the portion of the charge trapping dielectric layer;

patterning the resist to form a plurality of resist features having respective first spacings therebetween;

performing a pocket implant through the first spacings and the portion of the charge trapping dielectric layer, the pocket implant performed at an angle relative to the semiconductor substrate so as to establish pocket implants within the substrate that extend at least partially under the resist features;

performing a bitline implant through the first spacings and the portion of the charge trapping dielectric layer to establish buried bitlines within the substrate having a width corresponding generally to the first spacing, the bitlines not covering the portions of the pocket implants that extend under the resist features;

removing the patterned resist;

forming the remainder of the charge trapping dielectric layer over the portion of the charge trapping dielectric layer;

forming a wordline material over the remainder of the charge trapping dielectric layer; and

patterning the wordline material to form wordlines that overlie the bitlines.

2. The method of claim 1, wherein a channel is defined between two buried bitlines, the portions of pocket implants extending under the resist features changing doping within select portions of the channel.

3. The method of claim 1, wherein the bitline implant is performed before the pocket implant.

4. The method of claim 1, wherein forming a portion of a charge trapping dielectric layer comprises:

forming a first insulating layer over the semiconductor substrate; and

forming a charge trapping layer over the first insulating layer.

5. The method of claim 4, wherein forming the remainder of the charge trapping dielectric layer comprises:

forming a second insulating layer over the charge trapping layer.

6. The method of claim 5, wherein the first and second insulating layers comprise at least one of one or more silicon-rich silicon dioxide layers, one or more oxygen-rich silicon dioxide layers, one or more thermally grown or deposited oxide layers, materials having a high dielectric constant and one or more nitrided oxide layers.

7. The method of claim 5, wherein the charge trapping layer comprises at least one of one or more silicon-rich silicon nitride layers and one or more nitrogen-rich silicon nitride layers.

8. The method of claim 5, wherein the first insulating layer is formed to a thickness of about 70 Angstroms or less.

9. The method of claim 5, wherein the charge trapping layer is formed to a thickness of between about 60 to 80 Angstroms.

10. The method of claim 5, wherein the second insulating layer is formed to a thickness of about 100 Angstroms or less.

11. The method of claim 1, wherein the pocket implant is performed at an angle of between about 5 to 40 degrees relative to the substrate.

12. The method of claim 11, wherein the pocket implant includes boron.

13. The method of claim 12, wherein the bitline implant includes at least one of arsenic, phosphorous and antimony.

14. The method of claim 13, wherein the bitline implant is performed at a dose of between about 0.75E15 and 4E15 atoms/cm^2.

15. The method of claim 14, wherein the bitline implant is performed at an energy level of between about 40 to 100KeV.

16. The method of claim 1, wherein the wordlines are oriented at substantially right angles relative to the buried bitlines.

17. The method of claim 1, wherein the pocket implant is performed at an energy level of between about 10 to 100 KeV.

18. The method of claim 1, wherein the pocket implant is performed at a dose of between about 1E12 and 5E14 atoms/cm^2.

19. The method of claim 1, comprising:

performing a threshold adjustment implant into the semiconductor substrate prior to forming the portion of the charge trapping dielectric layer.

20. The method of claim 19, wherein the threshold adjustment implant includes boron.

21. A method of forming at least a portion of a SONOS dual bit memory core array upon a semiconductor substrate, the method comprising:

forming pocket implants within the substrate without patterning a first insulating layer overlying the substrate or a charge trapping layer overlying the first insulating layer, the pocket implants being implanted at least partially under features formed out a resist

material overlying the charge trapping layer and through the first insulating layer, the charge trapping layer and first spacings formed between the resist features;

forming bitline implants through the first spacings to establish buried bitlines within the substrate having respective widths corresponding generally to the first spacings, the bitlines not covering the portions of the pocket implants that extend under the resist features;

removing the resist features;

forming a second insulating layer over the charge trapping layer;

forming a wordline material over the second insulating layer; and

patterning the wordline material to form wordlines that overlie the bitlines.

22. The method of claim 21, wherein the first and second insulating layers comprise at least one of one or more silicon-rich silicon dioxide layers, one or more oxygen-rich silicon dioxide layers, one or more thermally grown or deposited oxide layers and one or more nitrided oxide layers.

23. The method of claim 21, wherein the charge trapping layer comprises at least one of one or more silicon-rich silicon nitride layers and one or more nitrogen-rich silicon nitride layers.

24. The method of claim 21, wherein the pocket implants are formed at an angle of between about 5 to 40 degrees relative to the substrate.

25. The method of claim 21, wherein the pocket implants are formed at an energy level of between about 10 to 100 KeV and a dose of between about 1E12 and 5E14 atoms/cm^2.

26. The method of claim 21, wherein the pocket implants are formed at a dose of between about 1E12 and 5E14 atoms/cm^2.

27. At least a portion of a SONOS dual bit memory core array formed upon a semiconductor substrate comprising:

a first insulating layer that is not patterned, and is formed over the substrate;

a charge trapping layer that is not patterned, and is formed over the first insulating layer;

a second insulating layer that is not patterned, and is formed over the charge trapping layer;

a pair of bitlines buried within the substrate and defining a channel there-between;

pocket implants implanted into the substrate, the bitlines covering some of the pocket implants and some of the pocket implants extending into the channel, the portions of the pocket implants extending into the channel changing doping within select portions of the channel.